

Appln No. 09/550,757

Amdt date October 15, 2003

Reply to Office action of July 24, 2003

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

*Sub Ck7* 1-29. (Cancelled)

30. (Currently Amended) A ramping circuit assembly comprising:  
an input port configured to receive at least one decision feedback filter tap coefficient from a decision feedback filter;  
a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a predetermined first value to a second value, the second value being dependent upon a the at least one decision feedback filter tap coefficient; and  
an output port configured to communicate information representative of the ramped output(s) to a precoder.

31. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

32. (Original) The ramping circuit assembly as recited in claim 30, wherein the information representative of the ramped values comprises a difference between a present value of a tap

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coefficient of the precoder and a new value of the tap coefficient of the precoder.

33. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped generally linearly.

34. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped non-linearly.

35. (Original) The ramping circuit assembly as recited in claim 30, wherein the ramped output is ramped generally exponentially.

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36. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

37. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a transmitter.

*Sub C97*  
38. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

39. (Original) The ramping circuit assembly as recited in claim 30, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

40. (Currently Amended) A receiver comprising:  
a decision feedback filter;

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a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from the decision feedback filter;

a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a predetermined first value to a second value, the second value being dependent upon a the least one of the decision feedback filter tap coefficient; and

an output port configured to communicate information representative of the ramped output(s) to a precoder.

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41. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

42. (Original) The receiver as recited in claim 40, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

43. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped generally linearly.

44. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped non-linearly.

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45. (Original) The receiver as recited in claim 40, wherein the ramped output is ramped generally exponentially.

46. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

47. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a transmitter.

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C87 48. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

49. (Original) The receiver as recited in claim 40, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

50. (Currently Amended) A transmitter comprising:  
a precoder;  
a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from a decision feedback filter;

a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the varied output being ramped over time from a predetermined first value to a second value, the second value

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being dependent upon a the at least one decision feedback filter tap coefficient; and

an output port configured to communicate information representative of the ramped output(s) to the precoder.

51. (Original) The transmitter as recited in claim 50, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

52. (Original) The transmitter as recited in claim 50, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

53. (Original) The transmitter as recited in claim 50, wherein the ramped output is ramped generally linearly.

54. (Original) The transmitter as recited in claim 50, wherein the ramped output is ramped non-linearly.

55. (Original) The transmitter as recited in claim 50, wherein the ramped output is ramped generally exponentially.

56. (Original) The transmitter as recited in claim 50, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

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57. (Original) The transmitter as recited in claim 50, wherein the coefficient ramping circuit is configured to define a portion of a transmitter.

58. (Original) The transmitter as recited in claim 50, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

59. (Original) The transmitter as recited in claim 50, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

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com* 60. (Currently Amended) A transceiver comprising:  
a decision feedback filter;  
a precoder;  
a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from the decision feedback filter;

a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a first predetermined value to a second value, the second value being dependent upon a the at least one decision feedback filter tap coefficient; and

an output port configured to communicate information representative of the ramped output(s) to a precoder of a complimentary transceiver.

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61. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

62. (Original) The transceiver as recited in claim 60, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder of the complimentary transceiver and a new value of the tap coefficient of the precoder of the complimentary transceiver.

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63. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped generally linearly.

64. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped non-linearly.

65. (Original) The transceiver as recited in claim 60, wherein the ramped output is ramped generally exponentially.

66. (Original) The transceiver as recited in claim 60, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

67. (Original) The transceiver as recited in claim 60, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

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68. (Currently Amended) A transceiver comprising:

a decision feedback filter;

a precoder;

a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from a decision feedback filter of a complimentary transceiver;

a coefficient ramping circuit configured to provide a ramped output for at least one of the tap coefficients of the complimentary decision feedback filter, the ramped output being varied over time from a first predetermined value to a second value, the second value being dependent upon the tap coefficient of the complimentary decision feedback filter; and

an output port configured to communicate information representative of the ramped output(s) to the precoder.

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69. (Original) The transceiver as recited in claim 68, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a feedback filter tap coefficient.

70. (Original) The transceiver as recited in claim 68, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

71. (Original) The transceiver as recited in claim 68, wherein the ramped output is ramped generally linearly.

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72. (Original) The transceiver as recited in claim 68, wherein the ramped output is ramped non-linearly.

73. (Original) The transceiver as recited in claim 68, wherein the ramped output is ramped generally exponentially.

74. (Original) The transceiver as recited in claim 68, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

75. (Original) The transceiver as recited in claim 68, wherein the coefficient ramping circuit is configured to define a portion of a transmitter.

76. (Original) The transceiver as recited in claim 68, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

77. (Original) The transceiver as recited in claim 68, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

78. (Currently Amended) A communication system comprising:  
at least two transceivers, each transceiver comprising:  
    a decision feedback filter;  
    a precoder;  
    a ramping circuit assembly, the ramping circuit assembly comprising:  
        an input port configured to receive at least one decision feedback filter tap coefficient from the decision feedback filter;

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a coefficient ramping circuit configured to provide a ramped output for at least one of the decision feedback filter tap coefficients, the ramped output being varied over time from a first predetermined value to a second value, the second value being dependent upon a decision feedback filter tap coefficient; and

an output port configured to communicate information representative of the ramped output(s) to a precoder of a complimentary transceiver.

79. (Original) The communication system as recited in claim 78, wherein the ramped output is ramped from a value of approximately zero to a value approximately equal to a value of a filter tap coefficient.

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cont*

80. (Original) The communication system as recited in claim 78, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder of the complimentary transceiver and a new value of the tap coefficient of the precoder of the complimentary transceiver.

81. (Original) The communication system as recited in claim 78, wherein the ramped output is ramped generally linearly.

82. (Original) The communication system as recited in claim 78, wherein the ramped output is ramped non-linearly.

83. (Original) The communication system as recited in claim 78, wherein the ramped output is ramped generally exponentially.

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84. (Original) The communication system as recited in claim 78, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

85. (Original) The communication system as recited in claim 78, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

86. (Currently Amended) A communication system comprising:  
at least two transceivers, each transceiver comprising:

a decision feedback filter;

a precoder;

a ramping circuit assembly, the ramping circuit assembly comprising:

an input port configured to receive at least one decision feedback filter tap coefficient from a decision feedback filter of a complimentary transceiver;

a coefficient ramping circuit configured to provide a ramped output for at least one of the tap coefficients of the complimentary decision feedback filter, the ramped output being varied over time from a first predetermined value to a second value, the second value being dependent upon the tap coefficient of the complimentary decision feedback filter; and

an output port configured to communicate information representative of the ramped output(s) to the precoder.

87. (Original) The communication system as recited in claim 86, wherein the ramped output is ramped from a value of

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approximately zero to a value approximately equal to a value of a filter tap coefficient.

88. (Original) The communication system as recited in claim 86, wherein the information representative of the ramped values comprises a difference between a present value of a tap coefficient of the precoder and a new value of the tap coefficient of the precoder.

89. (Original) The communication system as recited in claim 86, wherein the ramped output is ramped generally linearly.

90. (Original) The communication system as recited in claim 86, wherein the ramped output is ramped non-linearly.

91. (Original) The communication system as recited in claim 86, wherein the ramped output is ramped generally exponentially.

92. (Original) The communication system as recited in claim 86, wherein the coefficient ramping circuit is configured to define a portion of a receiver.

93. (Original) The communication system as recited in claim 86, wherein the coefficient ramping circuit is configured to define a portion of a transmitter.

94. (Original) The communication system as recited in claim 86, wherein the coefficient ramping circuit is configured to define a portion of a DSL receiver.

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95. (Original) The communication system as recited in claim 86, wherein the coefficient ramping circuit is configured to define a portion of a DSL transmitter.

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Cancelled*  
96. (Canceled)

97. (Currently Amended) A message received by a communication device, the message being stored on a machine-readable media and containing information processed according to the method comprising precoding a signal to be transmitted with a precoder, the precoder having tap coefficients which are ramped over time from a first predetermined value to a second value, the second value being dependent upon a decision feedback filter tap coefficient.